

20 V, P-Channel FemtoFET™ MOSFET

Check for Samples: [CSD25483F4](#)

FEATURES

- Ultra-Low On Resistance
- Ultra-Low Q_g and Q_{gd}
- High Operating Drain Current
- Ultra-Small Footprint (0402 Case Size)
 - 1.0 mm x 0.6 mm
- Ultra-Low Profile
 - 0.35 mm Max Height
- Integrated ESD Protection Diode
 - Rated > 4 kV HBM
 - Rated > 2 kV CDM
- Pb-Free Terminal Plating and Halogen Free
- RoHS Compliant

APPLICATIONS

- Optimized for Load Switch Applications
- Optimized for General Purpose Switching Applications
- Battery Applications
- Handheld and Mobile Applications

DESCRIPTION

This 210 mΩ, 20 V P-Channel FemtoFET™ MOSFET is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing at least a 60% reduction in footprint size.

PRODUCT SUMMARY

V_{DS}	Drain-to-Source Voltage	–20	V
Q_g	Gate Charge Total (–4.5 V)	959	pC
Q_{gd}	Gate Charge Gate to Drain	161	pC
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = -1.8\text{ V}$	530 mΩ
		$V_{GS} = -2.5\text{ V}$	338 mΩ
		$V_{GS} = -4.5\text{ V}$	210 mΩ
$V_{GS(th)}$	Threshold Voltage	–0.95	V

ORDERING INFORMATION

Device	Qty	Media	Package	Ship
CSD25483F4	3000	7-Inch Reel	Femto(0402) 1.0 mm x 0.6 mm	Tape and Reel
CSD25483F4T	250		Land Grid Array (LGA)	

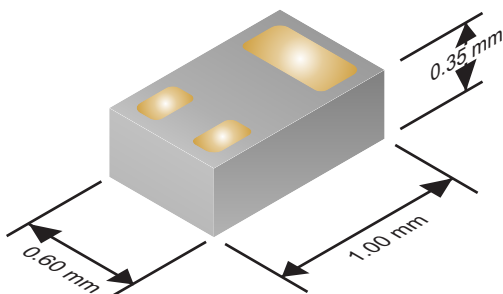
ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	–20	V
V_{GS}	Gate-to-Source Voltage	–12	V
I_D	Continuous Drain Current ⁽¹⁾	–1.6	A
I_{DM}	Pulsed Drain Current ⁽²⁾	–6.5	A
P_D	Power Dissipation ⁽¹⁾	500	mW
ESD Rating	Human Body Model (HBM)	4	kV
	Charged Device Model (CDM)	2	kV
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	$^\circ\text{C}$

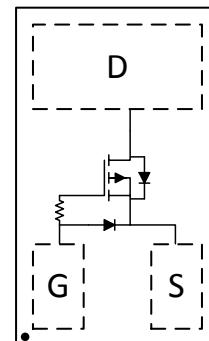
(1) Typical $R_{\theta JA} = 85^\circ\text{C/W}$ on 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Pulse duration $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

Typical Part Dimensions



Top View



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV _{DSS}	Drain-to-Source Voltage	V _{GS} = 0 V, I _{DS} = –250 μA	–20			V
I _{DSS}	Drain-to-Source Leakage Current	V _{GS} = 0 V, V _{DS} = –16 V	–1			μA
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = –12 V	–100			nA
V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{DS} = V _{GS} , I _{DS} = –250 μA	–0.70	–0.95	–1.20	V
R _{DS(on)}	Drain-to-Source On Resistance	V _{GS} = –1.8 V, I _{DS} = –0.1 A		530	1070	mΩ
		V _{GS} = –2.5 V, I _{DS} = –0.5 A		338	390	mΩ
		V _{GS} = –4.5 V, I _{DS} = –0.5 A		210	245	mΩ
		V _{GS} = –8 V, I _{DS} = –0.5 A		175	205	mΩ
g _{fs}	Transconductance	V _{DS} = –10 V, I _{DS} = –0.5 A	1.4			S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{GS} = 0 V, V _{DS} = –10 V, f = 1 MHz	198			pF
C _{oss}	Output Capacitance		82			pF
C _{rss}	Reverse Transfer Capacitance		5.8			pF
R _G	Series Gate Resistance	V _{DS} = –10 V, I _{DS} = –0.5 A	20			Ω
Q _g	Gate Charge Total (4.5 V)		959			pC
Q _{gd}	Gate Charge Gate to Drain		160			pC
Q _{gs}	Gate Charge Gate to Source		252			pC
Q _{g(th)}	Gate Charge at V _{th}		122			pC
Q _{oss}	Output Charge	V _{DS} = –10 V, V _{GS} = 0 V	1081			pC
t _{d(on)}	Turn On Delay Time	V _{DS} = 0 V, V _{GS} = –4.5 V, I _{DS} = –0.5 A, R _G = 2 Ω	4.3			ns
t _r	Rise Time		3.7			ns
t _{d(off)}	Turn Off Delay Time		17.4			ns
t _f	Fall Time		7.0			ns
Diode Characteristics						
V _{SD}	Diode Forward Voltage	I _{SD} = –0.5 A, V _{GS} = 0 V	–0.75			V
Q _{rr}	Reverse Recovery Charge	V _{DS} = –10 V, I _F = –0.5 A, di/dt = 100 A/μs	1060			pC
t _{rr}	Reverse Recovery Time		7.5			ns

THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		Typical Values	UNIT
R _{θJA}	Thermal Resistance Junction to Ambient ⁽¹⁾	85	°C/W
	Thermal Resistance Junction to Ambient ⁽²⁾	245	°C/W

(1) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.

(2) Device mounted on FR4 material with minimum Cu mounting area.

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

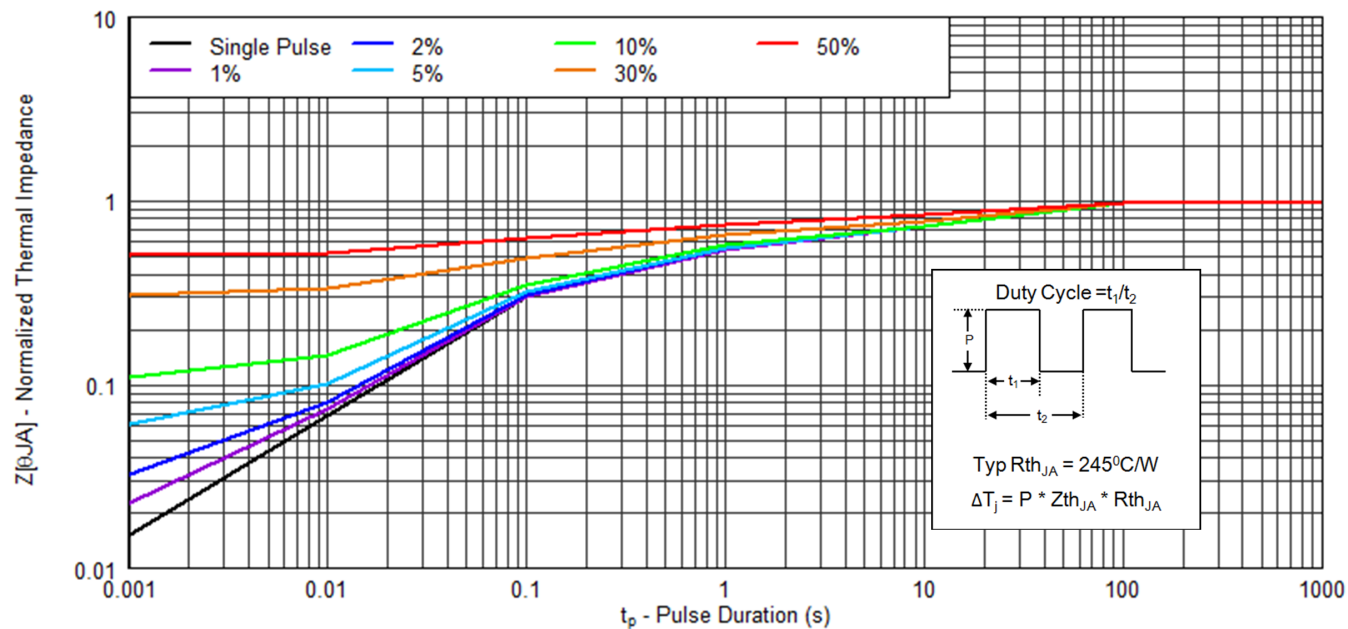


Figure 1. Transient Thermal Impedance

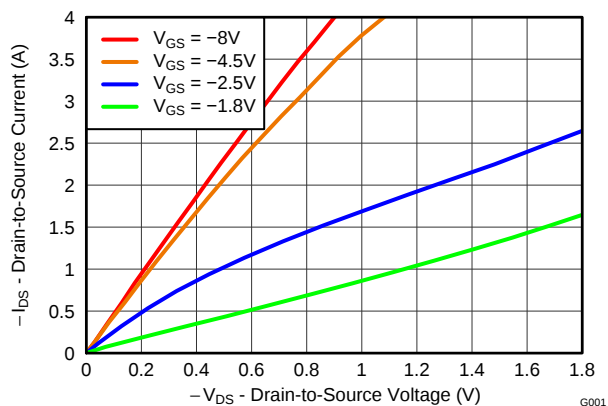


Figure 2. Saturation Characteristics

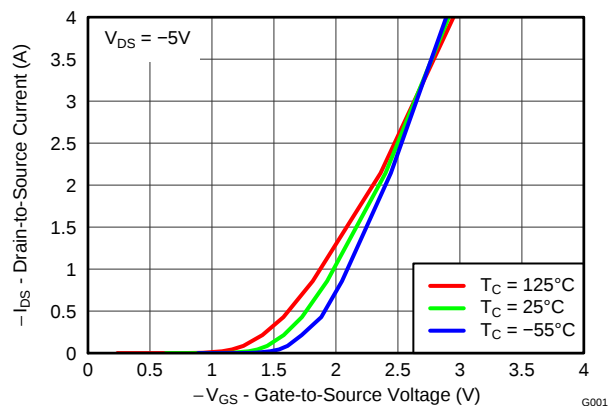


Figure 3. Transfer Characteristics

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

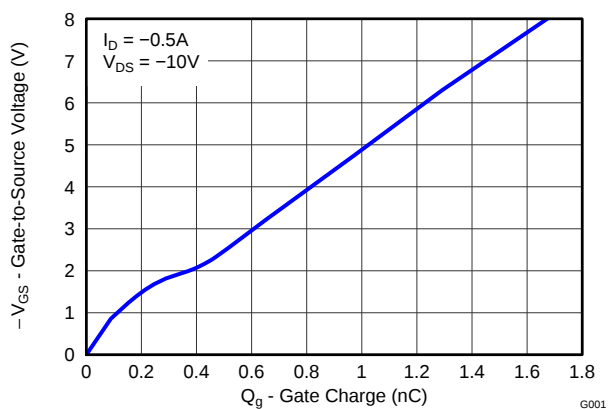


Figure 4. Gate Charge

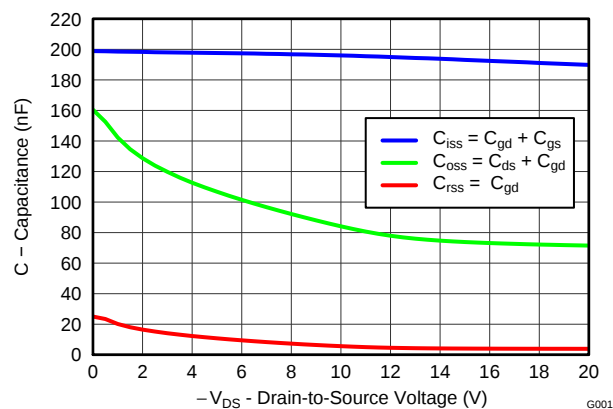


Figure 5. Capacitance

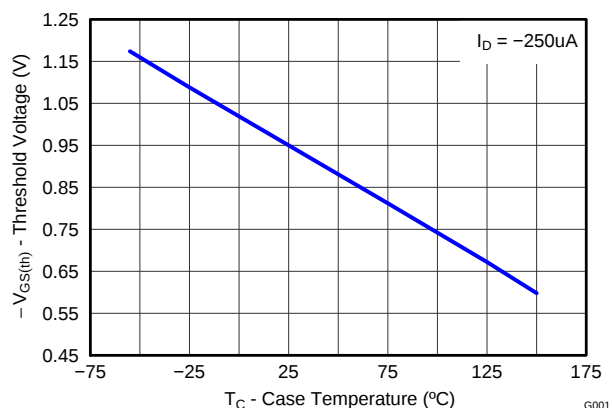


Figure 6. Threshold Voltage vs. Temperature

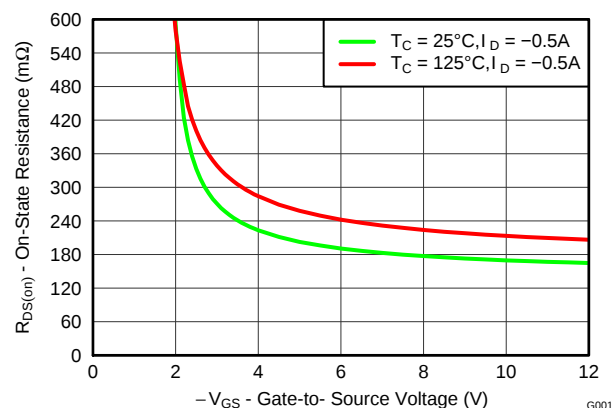


Figure 7. On-State Resistance vs. Gate-to-Source Voltage

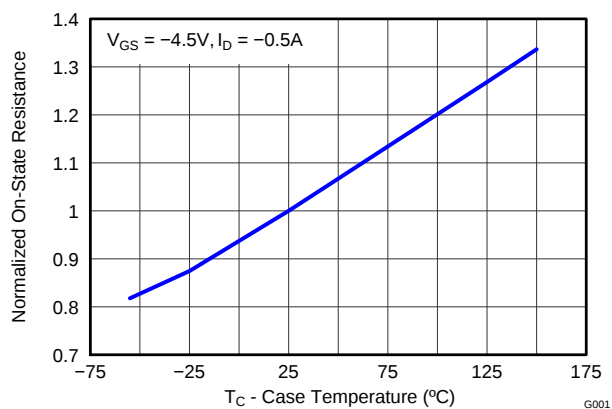


Figure 8. Normalized On-State Resistance vs. Temperature

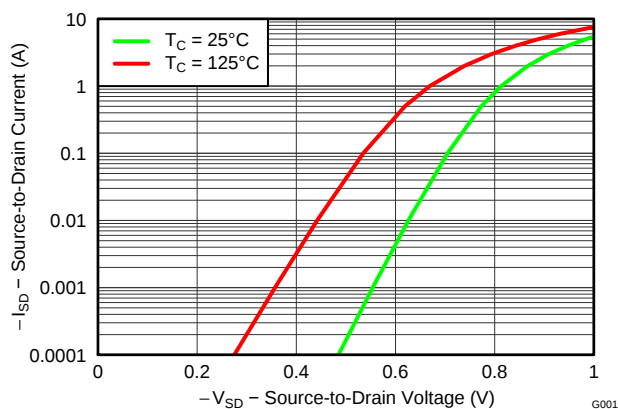


Figure 9. Typical Diode Forward Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

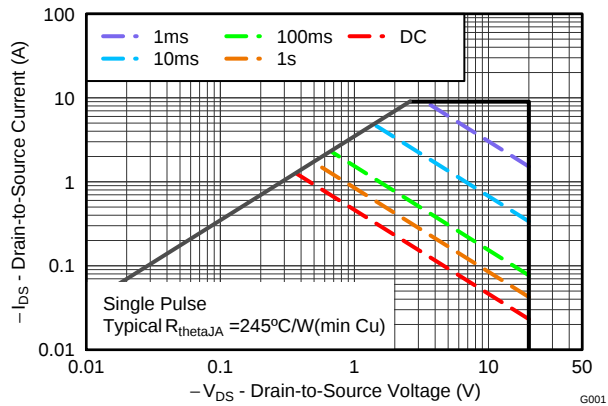


Figure 10. Maximum Safe Operating Area

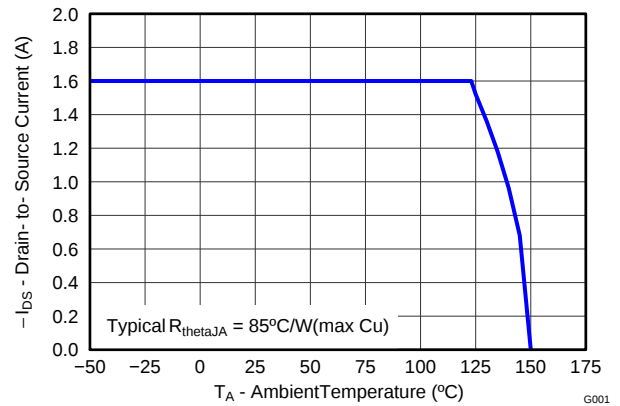
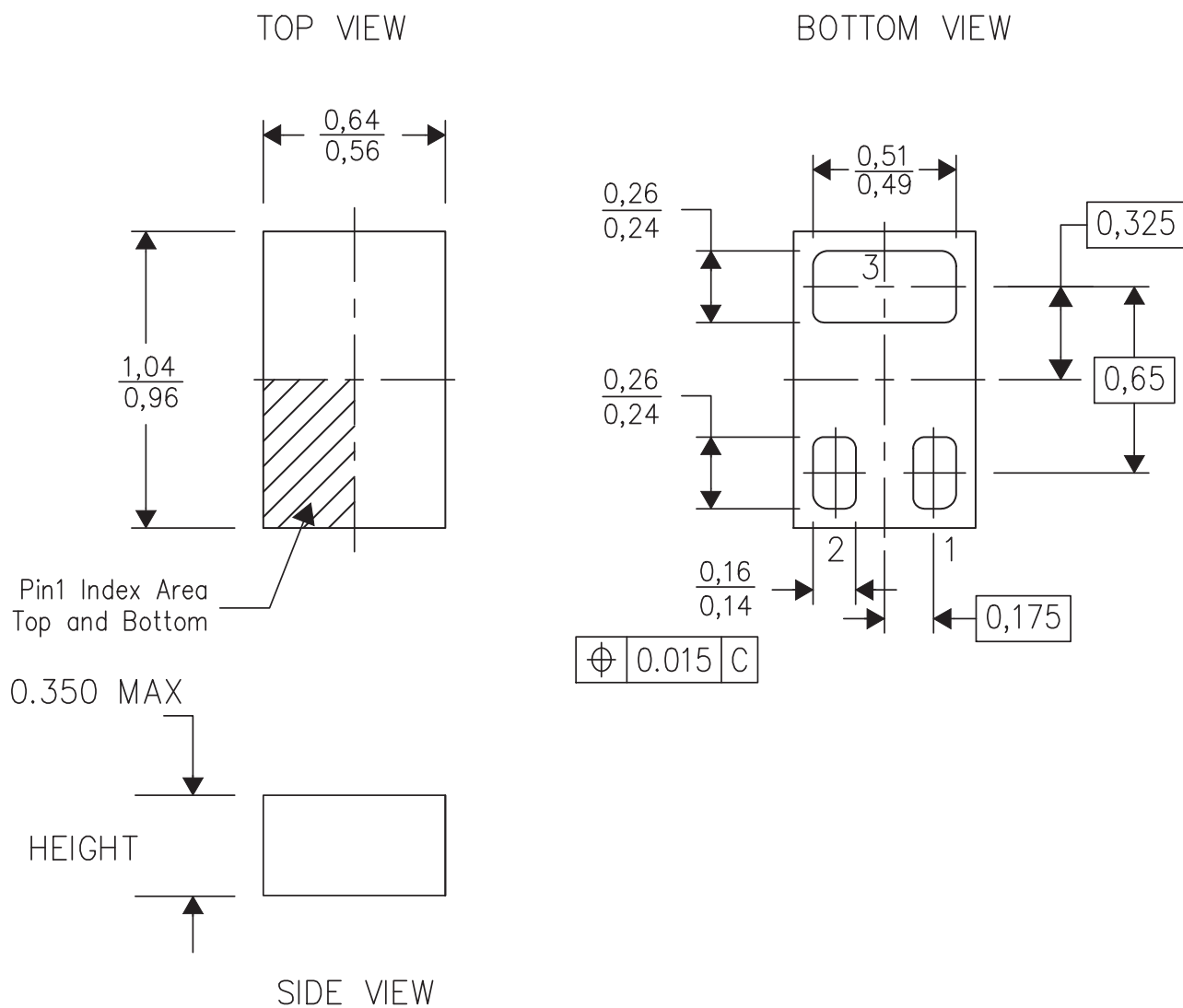


Figure 11. Maximum Drain Current vs. Temperature

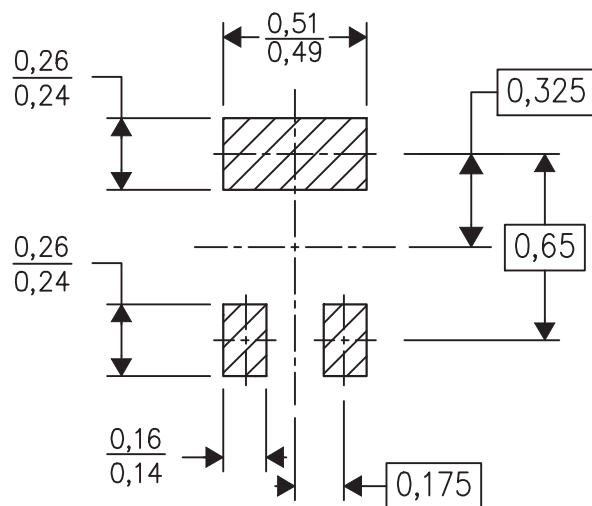
MECHANICAL DATA**0402 Mechanical Dimensions**

- (1) All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
- (2) This drawing is subject to change without notice.
- (3) This package is a PB-free solder land design.

Table 1. Pin Configuration

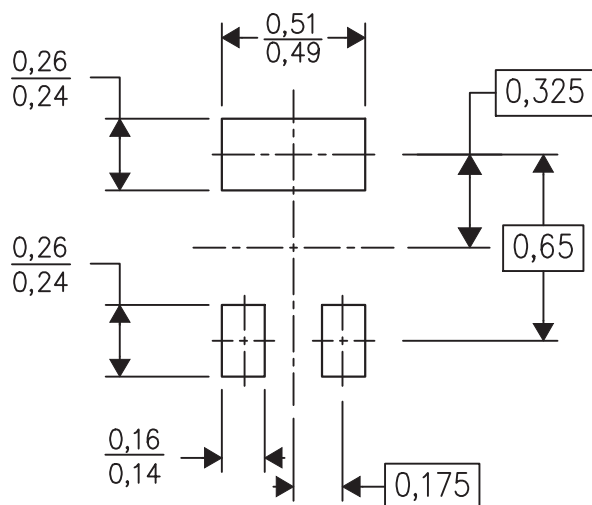
Position	Designation
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

Recommended Minimum PCB Layout



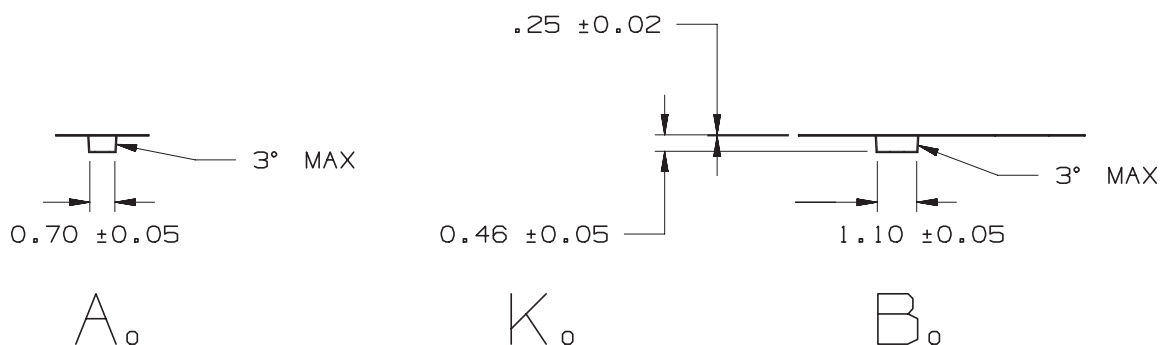
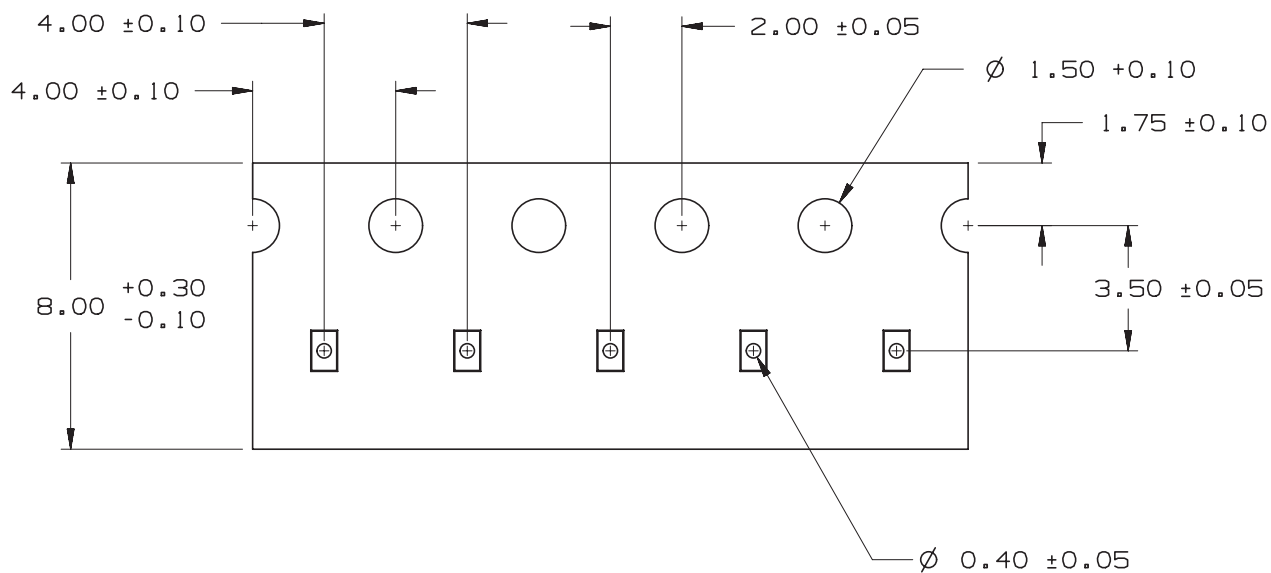
(1) All dimensions are in millimeters.

Recommended Stencil Pattern



(1) All dimensions are in millimeters.

CSD25483F4 Embossed Carrier Tape Dimensions



- (1) Pin 1 is oriented in the top-right quadrant of the tape enclosure (quadrant 2), closest to the carrier tape sprocket holes.

REVISION HISTORY

Changes from Original (October 2013) to Revision A	Page
• Updated title	1
• Fixed resistance typo	1
• Added small reel	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD25483F4	ACTIVE	PICOSTAR	YJC	3	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-250C-UNLIM	-40 to 85	DR	Samples
CSD25483F4R	PREVIEW	PICOSTAR	YJC	3	18000	TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

26-Nov-2013

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